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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,830	03/24/2004	Brian Taggart	ITL.1119US (P18791)	4317

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EXAMINER	
LEE, CALVIN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,830	TAGGART et al.	
	Examiner	Art Unit	
	Lee, Calvin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 08, 2005 (Amendment B)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-18 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Response to Amendment

1. The amendment of claims 1, 11 & 20 and the cancellation of claims 10, 19 & 29, received on July 08, 2005, are acknowledged.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains Patentability shall not be negatived by the manner in which the invention was made.

Note: This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3, 9, 11, 13-18, 20-21, and 23-28 are rejected under 35 U.S.C. 103(a) as unpatentable over *Babb et al* (US 6,569,508) in view of *Karnezos* (US 6,838,761).

Babb et al discloses a flexible packaged integrated circuit and its method comprising the step of securing a semiconductor die **68** within a cavity **58**, which is formed by at least two buildup layers **54**, **56** [Fig. 7] over a flexible substrate **70** of the flexible packaged circuit [col. 5, ln.59].

a) In re claims 1, 11-13, and 20-21, *Babb et al* does not suggest that the flexible substrate is folded, nor does suggest a folded package. Nevertheless, such folded substrate is known in the semiconductor art as evidenced by *Karnezos* disclosing the use of a flexible folding substrate, whereon a Z-interconnect is formed in a stacked module [Figs. 1-4].

It would have been obvious to one of ordinary skill in the art to modify the flexible substrate of *Babb et al* by utilizing a flexible folding substrate for the purpose of providing in principle for design flexibility [col. 2 in *Karnezos*].

b) In re claims 14-15 and 25-27, the combination of *Babb et al* and *Karnezos* teaches forming interconnection layers **42** [in Fig. 2] or **66** [in Fig. 7 of *Babb et al*] over the substrate and within the buildup layers [col. 5, ln.56].

c) In re claims 9 and 16, the combination of *Babb et al* and *Karnezos* also teaches the upper surface of the upper buildup layer being higher than the upper surface of the die [Fig. 5 in *Babb*].

d) In re claims 2, 17, and 23, *Babb et al* discloses a die attach or land pads **34**, **35** [in Fig. 2] or **62** [in Fig. 7], but not the lands coupled to solder balls and wire bonds. *Karnezos* suggests lands **141** and **143** coupled to solder balls **48** and wire bonds **16** [Fig. 4].

It would have been obvious to one of ordinary skill in the art to have modified the packaged integrated circuit of *Babb et al* by utilizing lands coupled to solder balls and wire bonds for the purpose of having a better electrical interconnect between interconnection layers and package die.

e) In re claims 3, 18, and 24, *Babb et al* suggests the substrate formed of polyester but not polyimide. *Karnezos* discloses [col. 2, ln.53] "various substrates may be used ... a flexible polyimide tape with 1-2 metal layers."

It would have been obvious to one of ordinary skill in the art to have modified the polyester substrate of *Babb et al* by utilizing a polyimide substrate for the purpose of possessing low expansion characteristics, ideally closer to that of a silicon chip, thereby improving reliability of the flip-chip connection under a cyclic temperature environment.

f) In re claim 28, the combination of *Babb et al* and *Karnezos* discloses a die attach or land pads **34**, **35** [in Fig. 2] or **62** [in Fig. 7 of *Babb et al*] over an adhesive layer **14**.

4. Claims 4-8, 12, and 22 are rejected under 35 U.S.C. 103(**a**) as unpatentable over *Babb et al* and *Karnezos*, as applied to claims 1, 11, and 20, in view of *Pendse* (US 5,468,994).

a) The combination of *Babb et al* and *Karnezos* is silent about a stepped cavity. *Pendse*, teaching the same semiconductor package device, discloses a flexible circuit **4** having a stepped cavity, wherein a semiconductor die **34** is attached to a substrate **22** [Fig. 5].

It would have been obvious to one of ordinary skill in the art to modify the packaged cavity of *Babb et al* by utilizing a stepped cavity, taught by *Pendse*, for the purpose of having a roomy cavity, whereon a die is formed with ease.

b) In re claims 5-6, the combination of *Babb et al*, *Karnezos*, and *Pendse* teaches forming interconnection layers **42** [in Fig. 2] or **66** [in Fig. 7 in *Babb et al*] over the substrate and within the buildup layers [col. 5, ln.56].

c) In re claim 7, the combination of *Babb et al*, *Karnezos*, and *Pendse* also teaches a die attach (or land or pad) coupled to solder balls and wire bonds, as shown in *Karnezos* [Fig. 4] lands **141** and **143** coupled to solder balls **48** and wire bonds **16**.

It would have been obvious to one of ordinary skill in the art to have modified the packaged integrated circuit of *Babb et al* by utilizing a die attach coupled to solder balls and wire bonds for the purpose of having a better electrical interconnect between interconnection(s) and package die.

d) In re claim 8, *Babb et al* teaches forming a die attach or land pads **34**, **35** [in Fig. 2] or **62** [in Fig. 7 of *Babb et al*] over the adhesive layer **14**. Moreover, *Karnezos* discloses a die attach epoxy **13** underlying a semiconductor die **14** [Fig. 1]. Alternately, *Pendse* [Fig. 5] discloses a die attach **36** between a die **34** and a substrate **22**.

Response to Arguments

5. After a closer review of the amended claims and after further search the related arts, the Examiner has found new pieces of art, US 6,838,761 to *Karnezos et al*, US 5,646,446 to *Nicewarner Jr. et al*, and US 5,436,744 to *Arledge et al*, which would read on at least the claims' amended feature –a folded flexible substrate. Therefore, the Allowance Subject Matter unfortunately has been replaced with a new Non-Final rejection clearly stated in detail above.

General Information

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: *Nicewarner, Jr. et al* (US 5,646,446) discloses a folded flexible substrate of integrated circuits [cols. 5-6]; and *Arledge et al* (US 5,436,744) discloses LCD and display electrodes formed on a folded flexible substrate [Fig. 1 and col. 3].

7. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30 (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The central fax number for the organization (where this application is assigned to) is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http://pair-direct.uspto.gov. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.

Calvin Lee

Dated: July 27, 2005